REMARKS

Claims 1-30 are all the claims presently pending in the application. The Examiner has withdrawn claims 25 and 26.

It is noted that the claim amendments, if any, are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicants specifically state that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Applicants gratefully acknowledge that claims 6, 16, 18, and 22 would be allowable if rewritten in independent form. However, Applicants respectfully submit that all of the claims are allowable.

Claim 14 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 1-5, 7, 9, 12, 14, 19, 24, and 27-29 stand rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,084,295 to Horiuchi et al. Claim 23 stands rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,294,897 to Notani et al.

Claim 8 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiuchi, further in view of US Patent Publication US 2004/0182911A1 to Chia et al. Claims 10 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiuchi, further in view of US Patent 3,840,169 to Steranko et al. Claim 13 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiuchi, further in view of US Patent Publication US 2001/00154900A1 to Lee.

Claims 15, 17, and 30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiuchi, further in view of Notani et al. Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiuchi, further in view of US Patent 4,555,052 to Kurtz et al. Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Horiuchi, further in view of Lee.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

As described and defined in, for example, claim 1, the present invention is directed to a method of making an electronic interconnection. For a signal line to be interconnected, a plurality of bonding wires is used in a configuration that provides a controlled impedance effect.

The conventional method of wire bonding, as described on page 2 of the specification, beginning at line 2, inherently represents a parasitic inductance that limits bandwidth signals when a single bonding wire is used for a signal. This problem has been addressed in various methods, including the use of flip chip and ball grid concepts or filling the transition region with a high dielectric constant material such as an epoxy containing a ceramic. However, these conventional methods are not always applicable and can be expensive to implement.

The claimed invention, on the other hand, introduces the entirely different concept of using a plurality of bonding wires for a specific signal. By appropriately configuring this plurality of bonding wires, the plurality of bonding wires provides a controlled impedance effect for that specific signal line. In practice, for any given signal connection, a typical configuration might use one bonding wire to carry the signal current and the other bonding wire to carry the return current, which can represent ground for a single ended signal and the complementary signal for a differential pair.

II. THE WITHDRAWAL OF CLAIMS 25 AND 26

The Examiner considers that claims 25 and 26 are withdrawn, presumably as addressing a non-elected invention. However, Applicants submit that this constructive withdrawal would not be proper unless and until the Examiner places on record an evaluation consistent with that outlined in the MPEP.

More specifically, as clearly stated in MPEP §806.01, it is the claimed subject matter that must be considered in the rationale for the restriction, and Applicants submit that such basic evaluation principle has not been followed in the Examiner's constructive withdrawal of claims 25 and 26, since the Examiner's rationale steps outside the claimed invention. That is, the Examiner is understood as alleging that the product, as described by these two claims, can be made by "lead frame or lead-less plural joint forming", and that such forming would satisfy the description of the product claims.

In response, Applicants respectfully direct the Examiner's attention to the single limitation in the product claim 25 as being substantially the same as the single limitation for claim 1. Therefore, it must be concluded that the Examiner considers that "lead frame or lead-less plural joint forming" somehow satisfies the plain meaning of the description in the product claim. Accordingly, it is submitted that the Examiner would have the burden of searching whatever subclasses describe the "lead frame or lead-less plural joint forming", in order to ensure that independent claim 1 is not likewise satisfied.

Stated slightly differently, if the restriction evaluation is confined to the description of the claimed product invention, Applicants submit that the evaluation of record does not follow the procedure outlined in the MPEP, since the "lead frame or lead-less plural joint forming" would clearly appear to be outside this description, absent some explanation not currently of record. Therefore, unless the Examiner places on record a reasonable example of how "lead frame or lead-less plural joint forming" satisfies the description of product claim 25, the initial burden of establishing a basis for restriction has not been met in accordance to the process outlined in MPEP §806.01.

Applicants request that, therefore, upon completion of prosecution of the method claims, the two product claims be re-evaluated for rejoinder, since the current restriction does not appear to be consistent with MPEP §806.01.

III. THE 35 USC §112, SECOND PARAGRAPH REJECTION

Claim 14 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite. More specifically, the Examiner considers that the claim wording is confusing because it "fails to point out whether applicant is claiming a combination of round wires and ribbon wire, a combination of only round wires, or a combination of only ribbon wires."

Claim 14 states: "The method of claim 1, wherein said bonding wires comprise a combination of at least one round bonding wire and at least one ribbon wire."

Applicants submit that, to a patent practitioner, this claim language is clearly intended to refer to configurations of the present invention having at least two bonding wires to form a combination for a specific signal line. If only two bonding wires are used, then one of the two is a round bonding wire and the other wire is a ribbon wire.

It is noted that the plain meaning of this claim language does cover embodiments in which more than two bonding wires are used, but the configuration must have at least one

round bonding wire and at least one ribbon wire to be considered covered by this claim language. There may be, for example, additional wires that are not round bonding wire and not a ribbon wire. Or, there may be more than one round bonding wire or more than one ribbon wire.

This claim does not cover the specific embodiment described by the Examiner in which there are only two or more round wires, since this configuration fails to include a ribbon wire, or the specific embodiment having only two or more ribbon wires, since this configuration fails to include a round wire. It is noted, however, that such configurations would be covered by the generic claim 1 and by generic claims 12 or 13.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

IV. THE PRIOR ART REJECTIONS

The Examiner alleges that Horiuchi anticipates claims 1-5, 7, 9, 12, 14, 19, 24, and 27-29 and that Notani anticipates claim 23. The Examiner also alleges that Horiuchi, when modified by Chia, renders obvious claim 8, when modified by Steranko, renders obvious claims 10 and 11, when modified by Lee, renders obvious claims 13, 21, and 30, when modified by Notani, renders obvious claims 15 and 17, and, when modified by Kurtz, renders obvious claim 20.

Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by Horiuchi. Moreover, it is submitted that the rejection currently of record fails to meet the initial burden of a *prima facie* rejection, since the plain meaning of the independent claims is clearly not satisfied, as that language would be understood by one having ordinary skill in the art, and as required by the Court in *Rexnord Corp. v. Laitram Corp.*, 274 F.3d 1336, 1342, 60 USPQ2d 1851, 1854 (Fed. Cir. 2001) and described in MPEP §2111.01: "*When not defined by applicant in the specification, the words of a claim must be given their plain meaning. In other words, they must be read as they would be interpreted by those of ordinary skill in the art.*"

More specifically, taking claim 1 as an example, the plain meaning of the claim language requires that a plurality of bonding wires be used for a specific signal line being interconnected. That is, the claim language clearly requires that at least two bonding wires be used for a single signal line. It is also required that the plurality of bonding wires is "

"configured to provide a controlled impedance effect". This latter description means, to one having ordinary skill in the art, that the claimed invention requires more than merely having two or more bonding wires or even having two or more bonding wires for a specific signal line, since it requires that the two or more bonding wires must also provide the effect of the controlled impedance.

Applicants submit that the technique in Horiuchi (or, for that matter, any of the prior art currently of record) fails to satisfy this description, since there is no signal line that is configured to have at least two bonding wires to conduct that signal, let alone two bonding wires configured to provide a controlled impedance for the signal line.

Although the description at lines 29-33 of column 5 does mention impedance matching by selection of insulation material, this method of impedance matching does not satisfy the plain meaning of the claim language that requires that at least two bonding wires be used for a signal line. It is also noted that the description in lines 28-30 of column 5 mentions creating the impedance effect of a coaxial cable line, it also fails to satisfy the plain meaning of the claim language, since a grounded electroconductive resin, rather than a second bonding wire, is used to provide the impedance matching.

Stated slightly differently, Horiuchi shows, at most, a single wire, coaxial configuration in which the signal is carried by a wire but the return is carried by a surrounding conductive medium. The multiplicity of wires has nothing to do with controlling the impedance. The geometries addressed in Horiuchi address mechanical requirements imposed by either the substrate or the IC. There is no suggestion of tying performance of the wirebonds to their collective configuration, and, indeed, as mentioned above, the configurations of Horiuchi use a single wirebond per signal, whereas the claimed invention requires more than one, typically (at least) one wirebond to carry the signal and (at least) one wirebond to carry the return.

The geometries discussed in Horiuchi variously refer to a coaxial configuration for both the wirebond segment and, in a later elaboration, the vias in the substrate. In both cases, the thickness of the dielectrics and their dielectric constants affect the resulting impedance. Since the wires/vias are shielded from each other by the conductive medium which carries the return currents, their spacing is irrelevant, which is not the case for the present invention.

Along this line, although not covered by any claim, to assist the Examiner's understanding of the co-dispensing aspect of the present invention, Applicants include attachments hereinbelow. This aspect of the present invention relies upon precise control

wirebond-to-wirebond separation, which is facilitated by threading the wires through a single bonding tip. None of the prior art currently of record shows this type of co-dispensing at the close dimensions addressed by the present invention.

Hence, turning to the clear language of the claims, in Horiuchi there is no teaching or suggestion of: "A method of making an electronic interconnection, said method comprising: for a signal line to be interconnected, using a plurality of bonding wires configured to provide a controlled impedance effect", as required by independent claim 1. Other independent claims have similar language.

Thus, Applicants submit that there are elements of the claimed invention that are not taught or suggest by Horiuchi, and, since the rejection currently of record relies upon primary reference Horiuchi for all pending claims, all claims are clearly patentable over Horiuchi. Therefore, the Examiner is respectfully requested to withdraw the rejections based on this reference.

However, in an attempt to expedite prosecution by assisting the Examiner to better understand the differences between the present invention and the cited prior art, Applicants submit the following comments relative to the rejections for other claims.

Relative to claim 2, the Examiner alleges that "*Horiuchi further teaches predetermined distances between each wire and shows wires subsequently above each other in figure 1.*"

In response, Applicants submit that, to one having ordinary skill in the art, Figure 1 actually shows wires that occlude each other at the top of the arc and splay out at the chip and substrate termini. The present invention would not function well in this configuration, in which a constant separation is not maintained. Moreover, Horiuchi only maintains a regular configuration of the wires in order to meet a geometric requirement for connection to a regular array of connection points on the chip and/or substrate. This regular configuration does not aid, nor is it required to provide a controlled impedance effect in Horiuchi, as this is provided solely by the thickness and dielectric constant of the insulating dielectric and the bond wire diameter.

Relative to claim 3, the Examiner alleges that "... *Horiuchi shows wires in predetermined configuration alongside one another in figures 7(a) and 8.*"

In response, Applicants submit that, to one having ordinary skill in the art, the separations shown in Figure 7a, 7b, and 8 when compared to the diameter of the wires would be ineffective in providing any controlled impedance effect.

Relative to claim 4, the Examiner alleges that "... *Horiuchi discloses a ground potential of the signal wire and dielectric insulation.*"

In response, Applicants submit that, to one having ordinary skill in the art, actually, Horiuchi sets the conductive resin at ground potential, not the bond wire.

Relative to claim 5, the Examiner alleges that Horiuchi discloses "it is possible to make the impedance-matching as a signal line by the selection of material (dielectric constant) and /or thickness of the resin coating 32 covering the conductive wire."

In response, Applicants submit that column 5, lines 29-30, makes it clear what Horiuchi intends "... so that the respective bonding wires operate as a coaxial cable line ...." The selection of the dielectric properties and geometries for this coaxial configuration in Horiuchi do not follow the same formulas as would be required for the exemplary microstrip and/or coplanar waveguide configurations as outlined in the present invention. In particular, in Horiuchi's coaxial configuration, the separation between bond wires does not even enter into the formula for impedance. In various exemplary embodiments of the present invention, it is a key feature and a significant, if not even crucial, parameter.

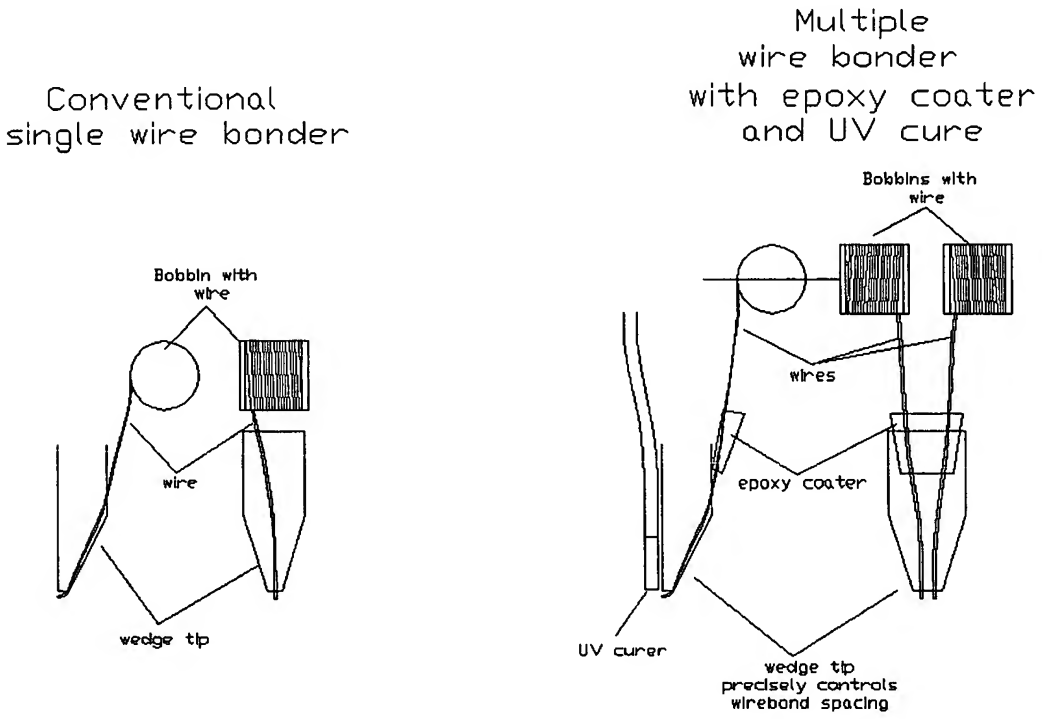
Relative to claim 7, Applicants submit that the language of this claim relates back to claims 1 and 5, which have been shown as clearly distinct from Horiuchi's environment.

Relative to claim 8, Chia might teach wirebonding using ultraviolet light-cured epoxies, but fails to suggest such use as would be required to overcome the deficiencies already identified for primary reference Horiuchi. That is, the present invention is not attempting to claim UV-cured epoxies coating wirebonds is novel.

However, Applicants submit that the use of UV-cured epoxy involved in several embodiments of the present invention is indeed novel, even if this element is already known in the art, since the rejection currently of record clearly demonstrates that it is not known in the combination of elements described by this claim.

Relative to claim 9, Horiuchi shows wires in a predetermined configuration. Figure 7a only shows wirebonds spaced regularly to meet the contact pitch of the substrate. This is an entirely different concept from that of the present invention and reinforces the observation that this method is only done to meet the mechanical requirements of the package, not to provide any impedance control function, since it is unlikely that the two spacings will coincide. Figure 8 shows a suggested cross-section for vias (plated through-holes) in the substrate which is irrelevant to the bond wire geometry discussed in our invention. Perhaps most significant, Horiuchi makes no suggestion to use more than one wire for a signal line.

Relative to the rejection for claims 10-11, Steranko states in the abstract: "circuits boards are positioned on a table, one circuit board beneath each of the heads...". This implies that the boards are separate entities. From the geometries in Steranko Fig 1, the wirebonds are clearly not in close proximity and it is not clear to Applicants how this technique can be extended in an obvious fashion to simultaneous bonding of wirebonds in the extremely close proximities that the present invention operates. The drawing below illustrates a preferred method for bonding wires in such close proximity, e.g.:



Relative to claims 12 and 14, although Horiuchi's figure 3 shows a round bonding wire, such round bonding wire fails to overcome the deficiency of claim 1.

Relative to claim 13, the ribbon bonding wire shown in Lee is similar to Notani in that both wire bonds are contacting the same electrode, which, in isolation, fails to achieve the effect described in independent claim 1. In exemplary embodiments of the present invention, one wire is used per electrode.

Relative to claims 15 and 17, the present invention does not replicate the structure of Notani, since the present invention does not place a ground conductor on the dielectric. This is a well known planar microstrip configuration. The present invention utilizes bond wires (which are usually suspended in air or embedded in epoxy) for the return current function

(which may be ground).

Relative to claim 19, Horiuchi is able to control impedance in the coaxial geometry shown therein by selecting dielectric constants, but this feature in isolation fails to overcome the deficiency for claim 1.

Relative to claim 20, the Examiner alleges that "Kurtz discloses ceramic as a dielectric material useful for electric insulation." Applicants submit that merely identifying ceramic as an electric insulation fails to satisfy the plain meaning of the claim language, as one having ordinary skill in the art would interpret this claim in conjunction with its antecedent claims.

Moreover, Applicants submit that the present invention relies upon ceramic for its high dielectric constant, not primarily for its insulating characteristic. It is further noted that the mention of ceramic in Kurtz's invention is incidental and has no functional relation to its use in the claimed invention. As such, Applicants submit that it would not be interpreted by one skilled in the arts as having an obvious connection with the claims.

Relative to claim 21, Applicants submit that Lee's patent discusses impedance matching to reduce insertion loss and to ameliorate the problems associated with reflections from impedance mismatching. It is implicit from his analysis that he is considering matching a common impedance on both termini of this structure as evidenced from the abstract "compared to the 50 ohm transmission line". The simpler case of impedance matching differs from the application of a filter where a particular response is being tailored (as opposed to a flat response) and differs from an impedance transformer which seeks to match different impedances on the respective termini.

Relative to claim 23, Notani shows a plurality (in his case, two) of bonding wires that are both connected to the same electrode and the reduction of parasitic effects requires additional components to achieve this effect. Therefore, Applicants submit that, to one having ordinary skill in the art, the two connectors 1a, 2b shown in Figure 1(a) do not satisfy the plain meaning of the language of this claim. It is further noted that the use of multiple wirebonds for this configuration in order to reduce overall inductance has a long history of application predating Notani. Merely decreasing inductance in a connector does not, by itself, achieve the result necessary to satisfy the plain meaning of the claim language.

Relative to claims 24 and 27, Horiuchi likewise fails to overcome the deficiencies identified for the parent claim.

Relative to the rejection for claim 28, although Horiuchi might reasonably be

described as disclosing electrically connecting a semiconductor chip to a connection on a circuit board, Applicants are not sure why simply showing the connection implies that impedances need to be matched per se. In many cases, impedances are deliberately mismatched between circuit nodes that are electrically connected in order to optimize performance.

Relative to claim 29, Applicants submit that Figures 8 and 9 in Horiuchi refer to the substrate geometry not to the bond wire, and are thus irrelevant.

Relative to claim 30, the Examiner alleges that Notani's invention extends a planar microstrip geometry in which "a strip signal conductor is disposed opposite a ground conductor on a dielectric substrate..." (col. 7, lines 2-3). In response, as mentioned previously, this is a conventional planar microstrip. In neither Horiuchi nor Notani is the concept of a wirebond carrying the ground (return) current disclosed.

Further, Applicants submit that the Examiner can point to no reasonable motivation or suggestion in the references that urge the combination as alleged by the Examiner. Indeed, in all urged combinations, the Examiner extracts lines from the secondary reference that are out of context from any reasonable direct relationship with the element being imported. As such, Applicants submit that the rejection of record clearly fails to satisfy the requirement in MPEP §2141.02: "*In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious*".

V. FORMAL MATTERS AND CONCLUSION

The Examiner objected to Figures 2A and 2B for failing to include description in the specification for label 207. Applicants have amended the specification to add description for this label and request that the Examiner reconsider and withdraw this objection.

In view of the foregoing, Applicant submits that claims 1-30, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 2/22/06

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